APPLICATION

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TITLE: DYNAMIC BUS REPEATER WITH IMPROVED NOISE TOLERANCE

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DYNAMIC BUS REPEATER WITH IMPROVED NOISE TOLERANCE

BACKGROUND

[0001] The length of interconnects between and within microprocessor data paths in functional unit blocks has increased as integration density has increased in integrated circuits (ICs). Because interconnect capacitance per unit length increases rapidly with lateral dimension scaling, long point-to-point interconnects may cause performance and power bottlenecks in ICs.

[0002] The substitution of dynamic CMOS interconnect drivers for static CMOS drivers in high performance on-chip busses has been explored. In busses with static drivers, when neighboring wires switch in the opposite directions, e.g., from Vss to Vcc on one wire and from Vcc to Vss on its neighbor, the voltage drop on the terminal of the parasitic capacitor between the two wires is not Vcc-Vss, but is doubled to (Vcc-Vss)*2. Due to the Miller effect, the effective capacitance seen by the wire is doubled, yielding a Miller Coupling Factor (MCF) of 2.0. In busses with dynamic drivers, all wires are reset to a pre-charge state (for example, Vss) in a pre-charge portion of the clock cycle, and then may either remain at that state or

switch to an opposite state (Vcc in this example) in an evaluate portion of the cycle. Thus two neighboring wires cannot switch in opposite directions from the pre-charge state, and the maximum voltage drop on the terminals of the parasitic capacitors between the two wires will be (Vcc-Vss). Thus, the MCF is reduced from 2.0 in static CMOS drivers to 1.0 in dynamic CMOS drivers, thereby reducing a large component of the wire's worst-case effective coupling capacitance. However, dynamic circuits tend to be more susceptible to noise than static circuits. This may not present a problem in circuits where the inputs are well shielded, but may present a problem in dynamic busses, where the distance from the driver and the large resistance of the interconnect isolate the end of a bus segment from its restoring impedance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1 is schematic diagram of a dynamic bus according to an embodiment.

[0004] Figure 2 is a circuit diagram of a dynamic driver according to an embodiment.

[0005] Figure 3 is a circuit diagram of a dynamic repeater according to an embodiment.

[0006] Figure 4 is an equivalent circuit diagram of the circuit diagram shown in Figure 3 at Vcc/2.

[0007] Figure 5 is a circuit diagram of a dynamic repeater according to an alternative embodiment.

[0008] Figure 6 is an equivalent circuit diagram of the circuit diagram shown in Figure 5 at Vcc/2.

DETAILED DESCRIPTION

[0009] Figure 1 illustrates a dynamic bus 100 according to an embodiment. The bus includes multiple bus lines 102. The bus lines may be arranged as domino data paths, each bus line including a dynamic driver 104 at the input 106, a series of inverting stages 108, each including a CMOS inverter 110 and a wire resistance 112, and a clocked flip flop (FF) 114 at the output 116. A dynamic bus repeater 120 in the middle of the bus line divides the bus line into a front segment 122 and a rear segment 124.

[0010] The driver 104 and the FF 114 are clocked by a $\Phi 1$ clock. The dynamic repeater is clocked by a $\Phi 2$ clock. Each clock splits a clock cycle into a precharge phase and an evaluate phase. In the precharge phase, the output node of the circuits in the dynamic bus are "pre-charged" to Vcc or Vss (alternating between inverting stages). In the evaluate phase, the output node of each circuit is

conditionally charged to Vcc (or discharged to Vss) based on its input. Thus, during the evaluate phase each circuit will either transition between Vcc and Vss or be quiescent.

[0011] Figure 2 is a circuit diagram of an exemplary dynamic driver 200. The driver includes a domino gate 202 and an inverter 204. In the pre-charge phase, the Φ1 clock signal is LOW. PMOS transistor 206 is turned on, proving a path from Vcc, and NMOS transistor 208 is turned off, closing the path to Vss. This pulls intermediate node 210 HIGH, which is inverted to a LOW signal by the inverter 204. The LOW pre-charge signal propagates through the bus line, pre-charging the output nodes of the inverters 110, FF 114, and dynamic repeater 120.

[0012] In the evaluate phase, the Φ1 clock signal transitions HIGH, turning off the PMOS transistor 206 and turning on the NMOS transistor 208. If the data signal input to the driver is HIGH, an input NMOS transistor 214 turns on and opens a path to Vss through NMOS transistor 208, pulling the intermediate node 210 LOW, which is inverted to a HIGH signal at the output node 212. This HIGH data signal propagates through the bus line. If the input data signal is LOW, the input NMOS transistor is off, blocking the path to Vss. Consequently, the intermediate node 210 remains HIGH, and the output node remains LOW.

[0013] The dynamic repeater splits the bus line into front and rear segments. The Φ2 clock is timed so that the rear segment of the bus is pre-charging while the front segment evaluates, and vice versa. In this manner, the pre-charge signal generated at the output node of the dynamic driver during pre-charge does not have to propagate through the entire bus line before the driver can evaluate a data signal at its input. The dynamic repeater has a latching function that hides the pre-charge state of the front segment from the rear segment while the rear segment is evaluating.

[0014] The Φ2 clock signal is approximately an inversion of the Φ1 signal. However, there may be an overlap window to account for clock skew. Also, the Φ2 clock may be timed so that Φ2 goes HIGH and places the dynamic repeater in evaluate mode slightly before the data signal from the front segment reaches the input node of the repeater. During the period between entering the evaluate mode and possibly receiving the data signal, the repeater is most susceptible to noise in the bus. If the noise exceeds the repeater's noise margin, the input transistor could switch, causing a false data signal to propagate down the rear segment of the bus line.

[0015] Dynamic bus repeaters may increase speed and decrease power consumption in the bus compared to static bus repeaters, but may be more susceptible to noise. Static inverters in busses can have a noise margin of about Vcc/2, i.e., a direct current (DC) input voltage of Vcc/2 produces an equal DC output voltage of Vcc/2. In a standard domino dynamic repeater, the noise margin may be only slightly higher than the threshold voltage, V_T, of the input transistor. While this may be acceptable for circuits where the inputs are well shielded, dynamic busses may be particularly susceptible to capacitive coupling and other sources of noise because the distance from of the repeater from the driver and the large resistance of the long interconnect isolate the repeater from its restoring impedance.

[0016] Figure 3 is a circuit diagram of a dynamic bus repeater 300 with an improved noise margin of about Vcc/2. The dynamic repeater includes a domino gate 302, an intermediate node 304, two pull-up PMOS transistors 306 and 308, a feedback inverter 310 and an output inverter 312. In this embodiment, the pre-charge state of the input node of the dynamic repeater is LOW (Vss). In an alternate embodiment, described in connection with Figure 5, the front segment includes an additional inverter stage, and

the pre-charge state of the input node of the dynamic repeater is HIGH (Vcc).

[0017] In the present embodiment, the intermediate node 304 is HIGH in the pre-charge state and the output node 314 is LOW. The repeater enters the evaluate mode when $\Phi 2$ goes HIGH, turning the top PMOS transistor 320 in the domino gate 302 OFF and turning the bottom NMOS transistor 322 ON. While the input node remains at the LOW pre-charge state, an input NMOS transistor 324 remains OFF, thereby maintaining the HIGH state of the intermediate node 304 and LOW state of the output node 314. Any noise signals at the input node of the dynamic repeater must exceed the noise margin of Vcc/2 for a sufficient amount of time to cause the input NMOS to turn ON, thereby providing a path to Vss and pulling the intermediate node LOW, consequently causing the output node to transition to a HIGH state.

[0018] The feedback inverter 310 provides an additional delay to switching in response to a noise signal. When a noise signal exceeds Vcc/2, the input NMOS transistor 324 starts to turn on, opening a path to Vss, and starts to turn off the lower pull-up PMOS transistor 306, closing the path to Vcc. As the path to Vcc begins to close and the path to Vss to open, the voltage on the intermediate node 304 begins to drop from HIGH to LOW. This signal starts to

activate the feedback inverter 310. After a sufficient amount of time, the signal at the node 340 at the input of the top pull-up PMOS transistor 308 would transition fully from LOW to HIGH, turning off the upper pull-up PMOS transistor and completely closing the path to Vcc. However, this feedback path produces a delay in closing the path to Vcc. Thus, the noise signal must exceed Vcc/2 for a sufficient amount of time to cause the output node to switch to a HIGH state.

[0019] While the rear segment of the bus is evaluating, the dynamic repeater hides the pre-charge signal propagating through the front segment from the rear segment. If the data signal was HIGH in the previous cycle, then the input NMOS transistor is ON, the intermediate node 304 is LOW, and the output node 314 is HIGH in the evaluate phase of that cycle. When the pre-charge signal for the present cycle reaches the input node 330, the LOW signal turns off the input NMOS transistor 324, and turns on the lower pull-up PMOS transistor 306. However, the LOW signal on the intermediate node 304 and inverted to a HIGH signal by the feedback inverter 310 maintains the upper pull-up PMOS in the OFF state, providing no path to Vcc. Thus, the intermediate node 304 remains LOW and the output node remains HIGH, thereby

hiding the pre-charge signal from the rear segment of the bus. If the data signal was LOW in the previous cycle, the LOW pre-charge signal will not change the state of bus, including the rear segment.

[0020] The transistors in the repeater must be sized to provide the circuit with a noise margin of Vcc/2. The pull-up PMOS transistors, the input transistor 324, and the bottom NMOS transistor 322 are sized in a ratio such that an equivalent circuit including these transistors, shown in Figure 4, has a noise margin of Vcc/2. With $\Phi 2$ HIGH, the top PMOS transistor is OFF and may be removed from the equivalent circuit. The feedback inverter 310 and output inverter 312 are static CMOS inverters, each with a noise margin of Vcc/2. Thus, with the output node of the repeater at Vcc/2 (the noise margin state), the input nodes of the output inverter and feedback inverter at intermediate node 304 and node 340, respectively, are also at Vcc/2. Since the inputs and outputs of the inverters are equal, they may be removed from the equivalent circuit. The remaining transistors in the equivalent circuit may be sized to achieve the noise margin state.

[0021] Figure 5 is a circuit diagram of an alternate embodiment of the dynamic repeater 500 in which the pre-charge state of the input node is HIGH. As described

above, the front segment may have one more (or less) inverting stage than the bus shown in Figure 1, thereby inverting the LOW pre-charge signal issued by the dynamic driver.

[0022] The dynamic repeater 500 includes a domino gate 502, an intermediate node 504, two pull-down NMOS transistors 506 and 508, a feedback inverter 510 and an output inverter 512. The upper PMOS transistor 520 and lower NMOS transistor 522 of the domino gate are clocked by the $\Phi 1$ clock. The timing scheme of the $\Phi 1$ clock is such that the repeater enters the evaluate mode slightly before the data signal from the first segment reaches the repeater. For example, the $\Phi 1$ clock signal to the dynamic driver may be delayed to achieve this timing condition.

[0023] In the present embodiment, the intermediate node 504 is LOW in the pre-charge state and the output node 514 is HIGH. The repeater 500 enters the evaluate mode when $\Phi 1$ goes LOW, turning top PMOS transistor 520 ON and turning the bottom NMOS transistor 522 OFF. While the input node remains at the HIGH pre-charge state, the input PMOS transistor 524 remains OFF, thereby keeping the path to Vcc closed and maintaining the LOW state of the intermediate node 504 and HIGH state of the output node 514. Any noise signals at the input node of the dynamic repeater must

exceed the noise margin of Vcc/2 for a sufficient amount of time to cause the input PMOS transistor 524 to turn ON, thereby providing a path to Vcc and pulling the intermediate node HIGH, consequently causing the output node to transition to a LOW state.

[0024] The circuit operates in a manner similar to the dynamic repeater shown in Figure 3, with NMOS pull-down transistors providing a path to Vss rather than Vcc. As described above, the feedback inverter provides an additional delay to the circuit.

[0025] While the rear segment of the bus is evaluating, the dynamic repeater hides the pre-charge signal propagating through the front segment from the rear segment. If the inverted data signal was LOW in the previous cycle, then the input PMOS transistor is ON, the intermediate node is HIGH, and the output node is LOW in the evaluate phase of that cycle. When the inverted (HIGH) pre-charge signal for the present cycle reaches the input node, the HIGH signal turns off the input PMOS transistor, and turns on the upper pull-down NMOS transistor. However, the HIGH signal on the intermediate node and inverted to a LOW signal by the feedback inverter maintains the lower pull-down NMOS in the OFF state, providing no path to Vss. Thus, the intermediate node remains HIGH and the output

node LOW, thereby hiding the pre-charge signal from the rear segment of the bus. If the inverted data signal was HIGH in the previous cycle, the inverted (HIGH) pre-charge signal will not change the state of bus, including the rear segment.

[0026] Figure 6 is an equivalent circuit of that shown in Figure 5 at the noise margin state and illustrates the transistors to size to achieve a noise margin of Vcc/2. In the present embodiment, the lower NMOS transistor 522 and inverters 510 and 512 drop out, and the upper PMOS transistor 520 and the input PMOS transistor 524 of the domino gate 502 and pull-down NMOS transistors 506 and 508 must be sized to achieve a noise margin of Vcc/2.

[0027] A number of embodiments have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, steps of the various operations may be performed in a different order and still achieve desirable results. Accordingly, other embodiments are within the scope of the following claims.